Design of an MRI quadrature-data acquisition card*

JIANG Zhongde**, ZU Donglin and GU Xiaofang

(Institute of Heavy Ion Physics, Beijing Key Laboratory of Medical Physics & Engineering, School of Physics, Peking University, Beijing 100871, China)

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Abstract A design of a quadrature-data acquisition card based on peripheral component interconnect (PCI) bus for mini-type magnetic resonance imaging (MRI) system is reported. It uses two high speed analog-to-digital converters (ADCs) to sample the MRI signals and two static random access memories (SRAMs) to store the data which will be read to the computer by PCI bus after sampling. All the logic control signals on the card are generated by the field programmable gate array (FPGA). The software Foundation3.1 is used to design the FPGA and achieve useful result after simulating and implementing. The card has some merits that normal commercial cards do not have. For example, the sampling parameters can be varied according to different pulse sequences.

Keywords: MRI, data acquisition, FPGA, PCI bus.

High speed data acquisition technique is developing very fast and used widely. A lot of commercial high speed data acquisition cards have appeared recently. However, these commercial cards are difficult to meet the requirements of MRI[1] system because they are not able to control the numbers of sampling points and do not have enough memory space and the cost is expensive. MRI system has its special requirements. For example, the number of sampling points and sampling interval should be set according to the different pulse sequences and the sampling frequency is determined by the bandwidth of sampling signals. The control of quadrature data acquisition is one of the kernel techniques. Data acquisition card is a hardware component and also is a bottom software component. Here we report the design of a high speed data acquisition card that meets MRI system requirements.

1 Operation and material

1.1 Quadrature demodulation

In radio communication technique, audio frequency signal can be extracted by demodulation and there is no necessity to use quadrature demodulation[1)]. However in MRI system, if using single channel demodulation, after digitizing MRI signal we can only obtain one real number matrix which is expressed as $\cos[\omega(x)t_x + \varphi(y)]$. A negative mirror frequency will appear in cosine function Fourier transform, thereby the spatial position of a pixel is uncertain if using these data to reconstruct an image, so as the sine function. If we use quadrature demodulation, we will obtain a complex number matrix expressed as $\cos[\omega(x)t_x + \varphi(y)] + i\sin[\omega(x)t_x + \varphi(y)]$. Using the complex matrix to reconstruct an image, the mirror frequency will disappear, consequently the spatial position of a pixel is unique. Fig. 1 shows a quadrature phase sensitive demodulation circuit.

1.2 MRI quadrature data acquisition system design

Fig. 2 shows the data acquisition system[2,3] design scheme. It consists of two ADCs, two SRAMs, one FPGA, one PCI bus controller (PCI9052[4]) and two operational amplifiers (OPA642) and so on. Two channel signals from phase sensitive detectors[5] (PSD) are converted by a pair of level conversion circuits and then enter into ADS804s. By analog-to-digital conversion, analog signals turn into digital data which are stored into SRAMs by the control of writing and address signals generated by the FPGA[6,7]. As soon as the data acquisition is ended, the FPGA will send a signal to computer, and then the sampled data in the SRAMs will be transported directly into the computer memory by the burst mode.

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** To whom correspondence should be addressed. E-mail: zhongdejiang@hotmail.com

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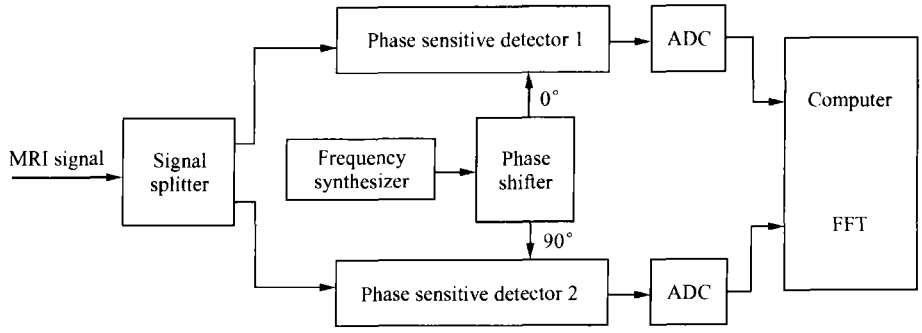

Fig. 1. MRI signal quadrature demodulation.

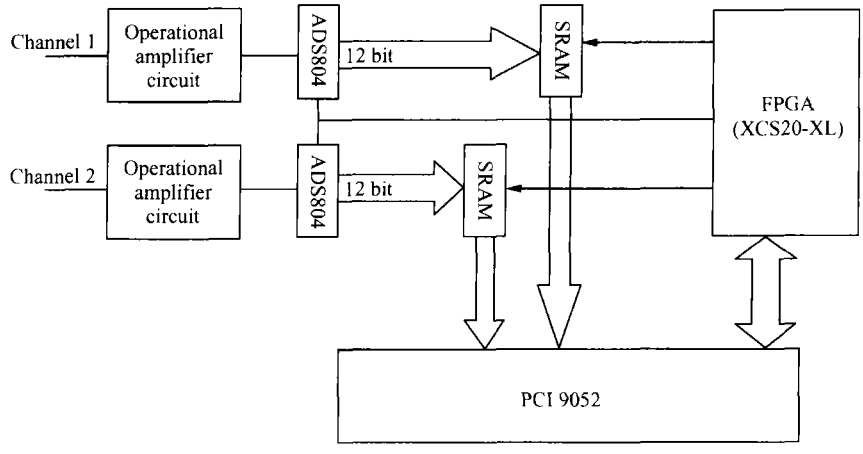

Fig. 2. Schematic diagram of data acquisition.

1.3 PCI bus controller PCI9052

The PCI bus protocol was put forward by Intel Inc. in 1992. PCI bus controller PCI9052 is PCI interface chip produced by PLX Inc., which is compliant with PCI2.1r. PCI9052's function can be divided into four logic areas: PCI interface logic, serial EEPROM interface logic, local bus interface logic and internal logic. By a serial EEPROM interface, PCI9052 accesses serial EEPROM which keeps the configuration information of PCI interface chip. During power-on, the PCI RST # signal resets the default values of the PCI9052 internal registers. In turn, the PCI9052 outputs the local LRESET # signal and checks for a serial EEPROM. If a serial EEPROM exists, and the first 48 bits are not all ones, the PCI9052 loads the internal registers from the serial EEPROM. Otherwise, default values are used.

1.4 Analog-to-digital converter ADS804

ADS804 produced by Burr-Brown Corporation is a 10 MHz, 12 bit pipelined analog-to-digital converter. ADS804 has a capability to set the input range in between $2V_{p\text{-}p}$ and $5V_{p\text{-}p}$ or to use external reference. Fig. 3 shows the sample timing diagram. From the diagram, we can know that sampling data will appear on output ports after six sample clocks from analog

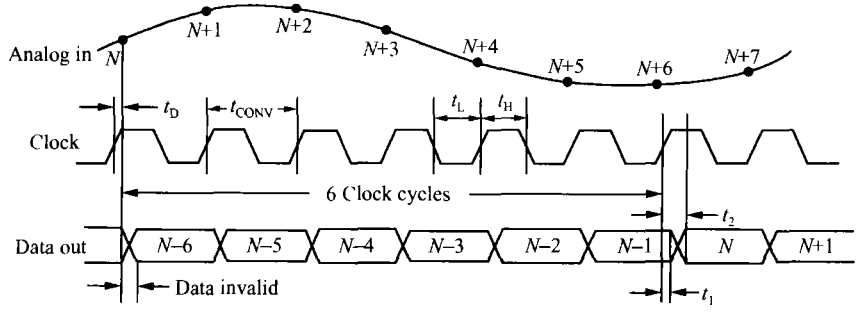

Fig. 3. ADS804 analog digital diagram.

signals enter ADS804. So the data have to be stored into SRAMs before the 7th sampling clock arrives, or it will be lost. We make use of FPGA to accomplish the exact delay to avoid the data loss.

1.5 SRAM

MRI sampling data are so large that they cannot be read in real time. There should be a SRAM to store the data before they are read by the computer. GVT72256A16-12[8] produced by GALVANTECh Inc. is chosen, whose access time is 12ns and memory space is 256 k * 16 Bytes.

1.6 FPGA

The appearance of CPLD/FPGA signs a revolution in the field of digital logic circuit design. It has the characteristic of static re-programmable and dynamic online reconfiguration, so the hardware can be designed and amended by program like the software. XCS20XL[9] of Xilinx Inc. is used in our design. It has 400 configurable logic blocks (CLBs), twenty thousands system gates and works at 3.3 V power supply. The CLBs are used to implement most of the logic in an FPGA. There are three look-up tables which are used as logic function generations, two flip-flops and two groups of signal steering multiplexers. During power down, FPGA will lose its configuration information. So generally configuration information is stored in the EEPROM (in our design we choose XC17S20XL as our EEPROM) which is compatible with FPGA. During power-up, the configuration information is loaded into FPGA under the control of logic circuit. There are three configuration modes: slave serial mode, master serial mode and express mode. In our design, we use master serial mode.

1.7 The software tool for development of digital logic circuit design

FPGA needs software tool to develop. Each FPGA corporation has its own development software such as Xilinx's ISE and Foundation, and Altera's Maxplux II and so on. Generally speaking there are six steps in FPGA design: design input, function simulation, design synthesis, design implement, timing simulation and device configuration. The first five steps are the course of design, debugging, optimization and validation. The 6th step is to generate a bit stream document and to download it into the FPGA.

2 Result

Fig. 4 shows the design of sampling logic circuit diagram in FPGA. We make use of a group of registers to store sampling parameters. ADSTART and RESET both come from the control register. RESET resets the sampling counter and the D-trigger. The fall edge of ADSTART triggers sampling. Sampling clock is derived from frequency divider. When the rise edge of sampling clock arrives, the sampling counter will plus one. Once the sampling counter's output is equal to the sampling comparator's input, the sampling comparator will output at a high level, which means having finished the sampling for a phase encode step. Address generator generates 18 bit addresses which are synchronous with sampling clock. There are many function modules in the design such as register groups, frequency divider, sampling timing control, sampling counter and so on. The design details and the simulation results are as the following.

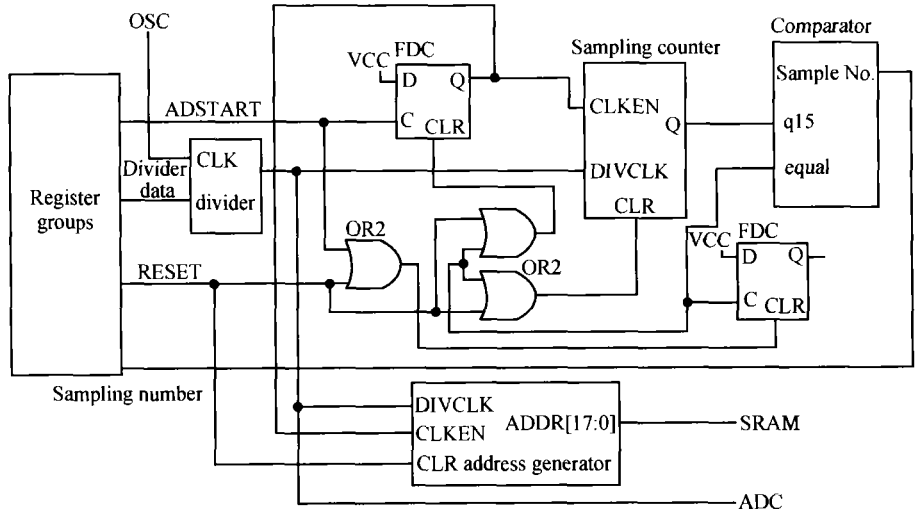

Fig. 4. Sampling logic circuit.

2.1 Register groups

Fig. 5 shows the configuration of the register groups. We have designed six 8-bit registers which respectively store the number of sampling points, the value of the divided frequency, the sampling control order, the sampling status and so on. For each sampling, the computer sets the initial values to these registers by I/O ports and also obtains the sampling status by reading the status register.

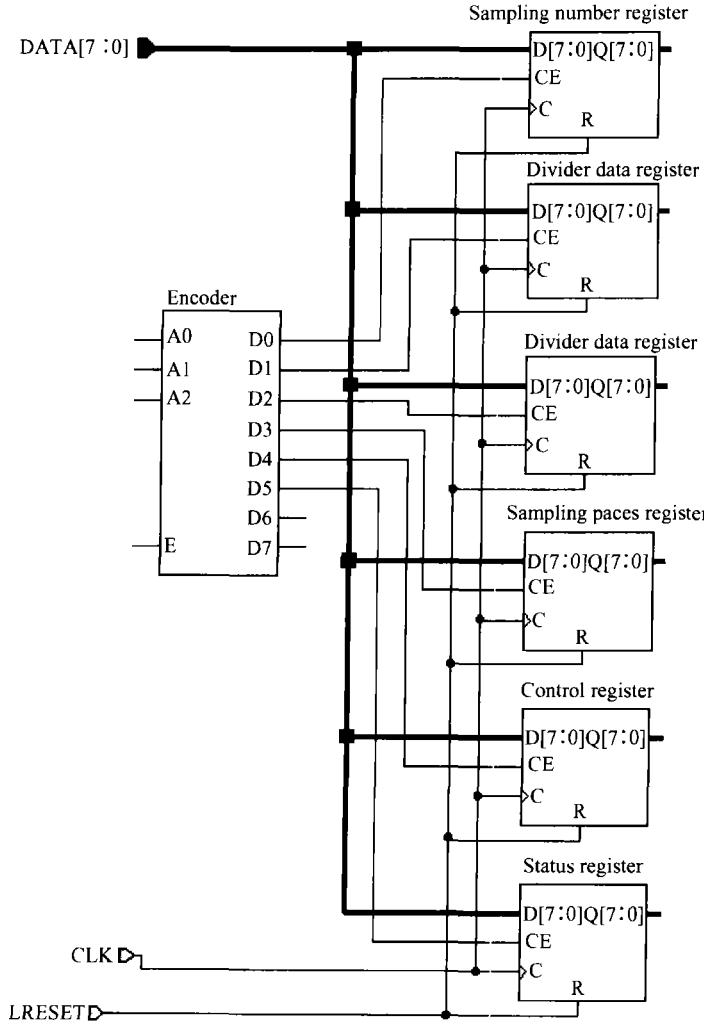

Fig. 5. Configuration of register groups.

2.2 Bus mastering

PCI9052 is the local bus controller. When writing data to FPGA, PCI9052 masters the control of the local bus. During sampling, FPGA requests the control of local bus by asserting LHOLD signal. If PCI9052 is not busy, it, by asserting LHOLDA, transfers the control of local bus to FPGA. When the sampling ends, PCI9052 gets back the control of local bus by de-asserting LHOLDA and then reads the sample data from SRAM.

2.3 Frequency divider

A frequency divider is to divide the clock frequency and outputs the sampling clock. The dividing data of the frequency which is set by the computer is of 16 bit. The sampling clock is defined as

$$Clock_{sample} = clock_{oscillator}/(2 * \text{dividing data} + 2)$$

Below is our VHDL[11] program for frequency divider.

```
if (clk'event and clk = '1') then
    if (divcnt = "1111111111111111") then
        divcnt <= divdata;
        divclk <= '1';
    else
        divcnt <= divcnt + 1;
        divclk <= '0';
    end if;
end if;
```

2.4 Function simulation of the sampling control logic

The sampling logic simulation is shown in Fig.6. The clk (50 MHz) is provided by the crystal oscillator under constant temperature. The adclk is the sampling clock which is derived from frequency divider (in Fig.6 the dividing data is 2). The sample number is the number of sampling points, set as 64. The sample step is the number of sampling steps. The adstart is the starting signal of sampling. The adstop is the stopping signal of sampling. The sramaddre is the address signal of SRAM. When sampling counter output, q15, reaches the initial sampling value, the adoe and the adstop will be at a high level while the sampling status bit of the status register also changes, which means that sampling of a phase encoding step is ended. Then computer can read the data from SRAM.

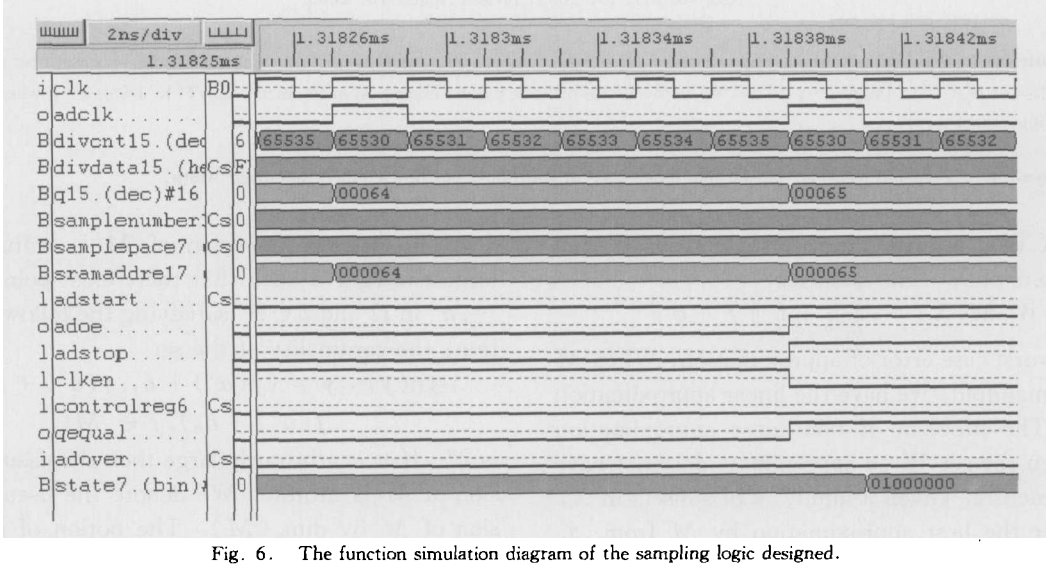

Fig. 6. The function simulation diagram of the sampling logic designed.

3 Conclusion and discussion

Although both XCS20XL and PCI9052 we chose for considering the cost are not the latest products in the present market, they can meet the demands of our mini-type MRI system. The PCI9052 configuration and the FPGA logic circuit design are of key importance. It is also important to make use of the software tool to develop the hardware. We have obtained some good simulation results by using Foundation3.1 in the design. This software has a GUI and is convenient to use. During programming, we can check the VHDL syntax at any time. The software can do the function simulation and the timing simulation after programming. The function simulation is to validate the system logic function, while timing simulation is to analyze time delay of the chip. So in order to meet time sequence, we need more time-delay circuits in the design.

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